FORM PTO - 1449 INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: CDS-006 APPLICANTS: Bellantoni et al. SERIAL NO.: 10/820,435 FILING DATE: 8-Apr-2004 GROUP: 2123

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
JP	A1	5,062,067	29-Oct-91	Schaefer et al.	364	578	15-Mar-89
	A2	5,437,037	25-Jul-95	Furuichi	395	700	7-Jun-93
	A3	5,502,661	26-Mar-96	Glunz	364	578	7-Oct-93
	A4	5,544,067	6-Aug-96	Rostoker et al.	364	489	14-Jun-93
	A5	5,696,942	9-Dec-97	Palnitkar et al.	395	500	24-Mar-95
	A6	5,768,567	16-Jun-98	Klein et al.	395	500	14-May-96
	A7	5,784,593	21-Jul-98	Tseng et al.	395	500	29-Sep-95
	A8	5,809,283	15-Sep-98	Vaidyanathan et al.	395	500	29-Sep-95
	A9	5,862,361	19-Jan-99	Jain	395	500	7-Sep-95
	A10	5,880,975	9-Mar-99	Mangelsdorf	364	578	5-Dec-96
	A11	5,978,571	2-Nov-99	Grundmann	395	500	12-May-97
	A12	5,991,523	23-Nov-99	Williams et al.	395	500.19	18-Mar-97
	A13	6,052,524	18-Apr-00	Pauna	395	500.43	14-May-98
	A14	6,134,516	17-Oct-00	Wang et al.	703	27	5-Feb-98
	A15	6,135,647	24-Oct-00	Balakrishnan et al.	395	500.19	23-Oct-97
	A16	6,152,612	28-Nov-00	Liao et al.	395	500	9-Jun-97
	A17	6,175,946 B1	16-Jan-01	Ly et al.	716	4	20-Oct-97
	A18	6,182,258 B1	30-Jan-01	Hollander	714	739	6-Feb-98
	A19	6,223,144 B1	24-Apr-01	Barnett et al.	703	22	24-Mar-98
	A20	6,295,517 B1	25-Sep-01	Roy et al.	703	15	7-Apr-98
	A21	6,321,363 B1	20-Nov-01	Huang et al.	716	4	11-Jan-99
JP	A22	6,466,898 B1	15-Oct-02	Chan	703	17	12-Jan-99

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FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
JP	C1	Andrews, J., Axis Systemss Inc., "Co-verification speeds SOC design," EDN, September 5, 2002, pp. 95-96, 98, 100.
	C2	Axis Systems, Inc, "Xpert™ ARM® Solution," Datasheet, www.AxisSystems.com, 2 pages.
	C3	Becker, M., "Faster Verilog Simulations Using a Cycle Based Programming Methodology," *Proceedings 1996 IEEE International Verilog HDL Conference*, Feb. 26-28, 1996, Santa Clara, CA, USA: IEEE Computer Society Press, 1996, pp. 24-31.
	C4	Bell, G., "Solidification – Static Functional Verification with Solidify," HDAC, Inc., 8 pages.
	C5	Björklund, D. et al., "A Language for Multiple Models of Computation," *Proceedings of the Tenth International Symposium on Hardware/Software Codesign*, May 6-8, 2002, Estes Park, CO, USA: CODES 2002, 2002 ACM, pp. 25-30.
	C6	Braun, G. et al., "Using Static Scheduling Techniques for the Retargeting of High Speed, Compiled Simulators for Embedded Processors from an Abstract Machine Description," *International Symposium on System Synthesis*, Sept. 30-Oct. 3, 2001, Montreal, Quebec, Canada: 2001 ACM, pp. 57-62.
	C7	Chatelain, A. et al., "High-Level Architectural Co-Simulation Using Esterel and C," *Proceedings of the Ninth International Workshop on Hardware/Software Codesign/CASHE*, April 25-27, 2001, Copenhagen, Denmark: 2001 ACM, pp. 189-194.
	C8	Choi, K. et al., "Incremental-in-time algorithm for digital simulation" Proceedings of the Design Automation Conference. Anaheim, June 12-15, 1988, Proceedings of the Design Automation Conference. Anaheim (DAC), New York, IEEE, US, vol. CONF. 25, 12-Jun-1988, pages 501-505.
JP	C9	Clarke, P., "Cambridge startup claims speedier simulation tools," *EE Times*, http://www.eetimes.com/story/OEG20000424S0041; April 24, 2000, 2 pages.

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OTHER ART, JOURNAL ARTICLES, ETC.

JP	C10	Clarke, P., "EDA tool generates bit- and cycle-accurate C code," *EE Times*, http://www.eetimes.com/story/OEG20010713S0069; July 13, 2001, 1 page.
	C11	Clarke, P., "Tenison tool draws Verilog into SystemC compilation," *EEdesign*, http://www.eedesign.com/article/showArticle.jhtml?articleID=17406761; December 18, 2000, 2 pages.
	C12	Creusillet, B. et al., "Interprocedural analyses of Fortran programs" Parallel Computing, Elsevier Publishers, Amsterdam, NL, vol. 24, no. 3-4, May 1998, pages 629-648.
	C13	DeVane, C. J., "Efficient circuit partitioning to extend cycle simulation beyond synchronous circuits" Computer-Aided Design, 1997. Digest of Technical Papers., 1997 IEEE/ACM International Conference on San Jose, CA, USA 9-13 Nov. 1997.
	C14	Donnelly, K., "High performance VHDL simulation using native compiled code" Electronic Engineering, Morgan-Grampian LTD. London, GB, vol. 65, no. 803, 01-Nov.1993, page 51, 53, 55, 57.
	C15	Duarte, D. et al., "Evaluating the Impact of Architectural-Level Optimizations on Clock Power," *Proceedings of the 14th Annual IEEE International ASIC/SOC Conference*, Sept. 12-15, 2001, Arlington, VA, USA: 2001 IEEE, pp. 447-451.
	C16	Edwards, C., "Two startups jump into co-verification," *EEdesign*, http://www.design.com/article/printableArticle.jhtml?articleID=17407943; September 23, 2002, 3 pages.
	C17	Edwards, C., "U.K.'s Celoxica, Tenison enter-co-verification fray," *Electronic Engineering Times*, October 14, 2002, pp. 24, 27.
	C18	Edwards, S. A., "Compiling Esterel into sequential code" Proc Des Autom Conf; Proceedings - Design Automation Conference 2000 IEEE, Piscataway, NJ, USA, 2000, pages 322-327.
	C19	French, R.S. et al., "A General Method for Compiling Event-Driven Simulations," Stanford University, http://suif.stanford.edu/papers/rfrench95/paper.html; 19 pages.
	C20	Greaves, D., Tenison Technology, "VTOC Verilog -> C," *International Workshop on Rapid System Prototyping*, Tenison TechEDA, www.tenisontech.com, pp. 1-12.
	C21	Gupta, S. et al., "Conditional Speculation and its Effects on Performance and Area for High-Level Synthesis," *International Symposium on System Synthesis*, Sept. 30-Oct. 3, 2001, Montreal, Quebec, Canada: 2001 ACM, pp. 171-176.
	C22	Hoffman, A. et al., "A Framework for Fast Hardware-Software Co-simulation," *Proceedings; Design, Automation and Test in Europe. Conference and Exhibition 2001*, Munich, Germany, March 13-16, 2001. IEEE Computer Society 2001, pp. 760-764.
JP	C23	International Search Report PCT/US 03/35649 dated 01-Dec-04

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OTHER ART, JOURNAL ARTICLES, ETC.

JP	C24	International Search Report PCT/US 03/35403 dated 14-Dec-04
	C25	International Search Report PCT/US 03/35508 dated 05-Jan-05
	C26	Iyer, A. et al., "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors," *Proceedings of the 29th International Symposium on Computer Architecture (ISCA '02)*, May 25-29, 2002, Anchorage, AK, USA: IEEE Computer Society 2002, pp. 158-168.
	C27	Joon-Seo, Yim, et al., "A C-based RTL Design Verification Methodology For Complex Microprocessor" Proceedings of the Design Automation Conference. Anaheim, June 9-13, 1997, New York, ACM, IS, vol. CONF. 34, 09-Jun-1997, pages 83-88.
	C28	Ju, Y-C, et al., "Incremental Circuit Simulation Using Waveform Relaxation" Proceedings of the ACM/IEEE Design Automation Conference. Anaheim, June 8-12, 1992, Proceedings of the ACM/IEEE Design Automation Conference (DAC), Los Alamitos, IEEE Comp. Soc. Press, US, vol. CONF. 29, 08-Jun-1992, pages 8-11.
	C29	Jung, Y. et al., "simCore: an event driven simulation framework for performance evaluation of computer systems" Modeling, analysis and simulation of computers and telecommunication systems, 2000. Proceedings. 8th International Symposium on San Francisco, CA, USA 29 Aug. - 1 Sept. 2002.
	C30	Kim, M.G. et al., "Implementation of a Cycle-Based Simulator for the Design of a Processor Core," *Proceedings of AP-ASIC '99: The First IEEE Asia-Pacific Conference on ASICs*, Aug. 23-25, 1999, Seoul, South Korea: 1999 IEEE, pp. 108-111.
	C31	Kravitz, S.A. et al., "Massively parallel switch-level simulation : A feasibility study" IEEE Inc. New York, US, vol. 10, no. 7, 01-Jul-97, pages 871-894.
	C32	Krishnaswamy, V. et al., "Parallel Compiled Event Driven VHDL Simulation" Conference Proceedings of the 1998 International Conference on Supercomputing ACM New York, NY, USA, July 1997, pages 297-304.
	C33	Kudlugi, M. et al., "Static Scheduling of Multiple Asynchronous Domains for Functional Verification," *DAC 2001*, June 18-22, 2001, Las Vegas, Nevada, USA: 2001 ACM, 6 pages.
	C34	Liu, J. et al., "Software Timing Analysis Using HW/SW Cosimulation and Instruction Set Simulator," *Proceedings of the Sixth International Workshop on Hardware/Software Codesign (CODES/CASHE '98)*, March 15-18, 1998, Seattle, Washington, USA: 1998 IEEE, pp. 65-69.
	C35	Maurer, P.M, "Scheduling Blocks for Heirarchical Compiled Simulation," Technical Report DA-23, 1991, VCAPP Laboratory, University of South Florida, ftp://pangolin.csee.usf.edu/pub/facul.ty/maurer/tech-reports/da23_91.pdf, 23 pages.
JP	C36	McCammon, R. et al., "Cycle-accurate model speeds design," *EE Times*, http://www.eetimes.com/story/OEG19990615S0021; November 13, 2002, 6 pages.

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OTHER ART, JOURNAL ARTICLES, ETC.

JP	C37	Palnitkar, S. et al., Sun Microsystems, Inc., "Cycle Simulation Techniques," *Proceedings of the 1995 IEEE International Verilog HDL Conference*, March 27-29, 1995, Santa Cruz, CA, USA: IEEE Computer Society Press, 1995, pp. 2-8.
	C38	Paul, J.M. et al., "Frequency Interleaving as a Codesign Scheduling Paradigm," *Proceedings of the Eighth International Workshop on Hardware/Software Codesign*, May 3-5, 2000, San Diego, CA, USA: CODES 2000, ACM 2000, pp. 131-135.
	C39	Schulz, S.E., "Timing analysis tools in the critical path have a crucial impact on the success of a design," *EEdesign*, http:// www.eedesign.com/editorial/2000/focusreport0008.html; November 13, 2002, 6 pages.
	C40	Stoye, W. et al., "Using Tenison VTOC™ for Large SoC Concurrent Engineering: A Real World Case Study," *GlobespanVirata*, TenisonEDA, www.tenison.com; pp. 1-13.
	C41	Sun Young Hwang, "Incremental algorithms for digital simulation" Integration, The VLSI Journal, North-Holland Publishing Company. Amsterdam, NL, vol. 7, no. 1, 01-Apr-1989, pages 21-34.
	C42	Tabbara, B. et al., "Fast Hardware-Software Co-Simulation Using VHDL Models," *Proceedings; Design, Automation and Test in Europe. Conference and Exhibition, 1999*, Munich, Germany, March 9-12, 1999. IEEE Computer Society 1999, pp. 309-316.
	C43	TenisonEDA, "Engineering Management in the SOC Era," www.tenison.com, 1 page.
	C44	TenisonEDA, "Hardware/Software Co-Design in the SOC Era," , www.tenison.com; pp. 1-7.
	C45	TenisonEDA, "Introducing VTOC™: Bridging the SOC Co-Development Gap," *Tenison EDA World Tour*, September 2002, www.tenison.com, 14 pages.
	C46	TenisonEDA, "VTOC 1.0 User Guide," www.tenison.com; pp. 1-51.
	C47	Tension Technology, "A Verilog to C Compiler," *Submitted to IEEE Transactions on Software Engineering*, pp. 1-10
	C48	Tenison Technology: Hardware & Software Working Together, "New cycle-based Verilog Compiler is 50 to 100 times faster than behavioural simulation," www.tenisontech.com\news\nw010302.htm; March 1, 2002, 1 page.
	C49	Tensilica, "Synopsys and Tensilica Partner to Provide New Cycle-Accurate Model Generation Platform, http://www.tensilica.com/html/pr_2000_05_24.html; November 13, 2002, 3 pages.
JP	C50	Ye, W. et al., "The Design and Use of SimplePower: A Cycle-Accurate Energy Estimation Tool," *Proceedings of the 37th Design Automation Conference*, Los Angeles, CA, USA: DAC 2000, 2000 ACM, pp. 340-345.

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